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INTEGRATED CIRCUIT DESIGN (PHASE II) BY JG NASH
HUGHES RESEARCH LAB.

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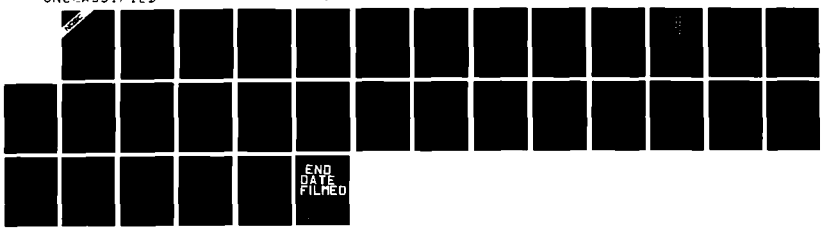

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NAVAL OCEAN SYSTEMS CENTER San Diego, California 92152-5000

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July 1987

Integrated Circuit Design (Phase II)

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Results of a study on the chip design of a low-power filter using state-of-the-art CMOS technology are described in this report. The filter is for speech applications and is specified to have 1024 taps with programmable weights and linear phase. The chip implementation is to have a word length of from 8 to 12 bits, and consume a maximum of 2.0 mA at 3.6 V. Reviewed are current capabilities of CMOS/SOS and CMOS/bulk technologies, and in particular, the Hughes VHSIC CMOS process. The architecture of the filter is discussed and estimates are made for the power consumption, speed, device count, and projected chip size of the filter implementation. A possible CMOS/SOS A/D circuit is also described.

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ILLUSTRATIONS

I. INTRODUCTION AND SUMMARY

This report is in response to a request to provide an analysis on the design of an ultra-low power integrated circuit which will perform digital filtering on voice bandwidth signals. This chip will contain a 1024-tap linear phase filter with programmable weights, operate at a sample rate of 8 kHz, and will consume a maximum of 7.2 mW power with a 3.6-volt power supply. This monolithic filter will contain: an 8-12-bit a/d, an internal processing clock oscillator, and the digital filter. This study only reports on the power requirements of the digital filter portion of the chip, although all portions must be considered in the overall power budget. Preliminary device count and die size estimates are presented. The work presented here is based on an earlier study performed by Hughes Research Laboratories (HRL) for NOSC [1]. Please refer to the summary section of this report for a concise statement of the findings.

A detailed transistor count and die size estimate will be generated in a future report. However, a preliminary estimate shows the die size to be in the neighborhood of 240 mils on a side. The preliminary device count is about 145k transistors. The following table summarizes the results of this analysis:

Power Consumption (digital section only)	5.8 mW
Projected Device Count	145,000 Tx
Projected Chip Size	240 x 240 mils

The power dissipation of the complete A/D circuit is summarized in the following table:

Source	Power (mW)
Comparator	2.024
PHI1 and Bit lines	.0134
Leakage	.00319
Capacitors	
Sample Mode	.09097
Redistribution Mode	.06064
Total	2.192 mW

Several global assumptions are made in this power dissipation analysis. Firstly, the output from the a/d is assumed to be in a 12-bit format. Secondly, the data samples are assumed to be in a sign-magnitude format so that an 11 x 11 multiplier may be used instead of a 12 x 12 multiplier. The sign-magnitude multiplier has superior area and power characteristics over a 2's complement multiplier. Thirdly, all circuit simulations for determining power dissipation were conducted by SLIC-M using nominal SOS III transistor model parameters at 25 degrees. Fourthly, SOS III (VHSIC-I) 1.25 μm design rules were used in conjunction with the device and interconnect capacitance values recommended by our modeling group to determine capacitive loading for power dissipation calculations [2]. Fifthly, all chip inputs and outputs are assumed to operate at CMOS levels. If TTL compatibility is desired, a power penalty would result from the DC current inherent in the TTL to CMOS input buffers. Lastly, an alternative architecture, described in Section II-A, is adopted permitting half the processing rate of the direct implementation Since power dissipation is directly related to the frequency of

operation, this alternative architecture will greatly reduce the power dissipation of the filter portion of this chip.

II. DETAILED ANALYSIS

A. Filter Architecture

The HRL report [1] advocated a single tap approach for the low power filter, based on its power dissipation advantages over alternative approaches. This filter performs the summation

$$y(n) = \sum_{m=0}^{1023} h(m)\ x(n-m) \qquad (1)$$

where $x(n)$ is the 12-bit filter digital input and $y(n)$ is the 12-bit filter digital output. Note that 1024 multiply-adds must be performed for each data sample, $x(n)$. Thus, a sample rate of 8 KHz will require a processing rate of 8.2 mHz. A 1024-word data RAM is required to store the incoming samples. Because of the linear phase requirement, $h(m)$ is symmetrical and thus only 512 coefficient samples need to be stored. The same coefficient, $h(m)$, is multiplied with two data samples, namely $x(n-m)$ and $x[n-(1023-m)]$. Therefore, the above summation may be equivalently expressed as:

$$y(n) = \sum_{m=0}^{511} h(m)\ \{x(n-m) + x[n-(1023-m)]\} \qquad (2)$$

Note that this equivalent summation requires that only 512 multiply-adds be performed for each data sample. Thus, a sample rate of 8 kHz will require a processing rate of 4.1 mHz, or one-half the processing rate of (1). Since power dissipation is proportional to frequency, the second summation, (2), is a more power efficient implementation.

A block diagram for this alternative approach is shown in Figure 1. This architecture is more complex than (1) and requires an additional 12-bit adder. Two 512-word data storage RAMs are required (same amount as (1)); one stores x(n-m) while the other stores x[n-(1023-m)]. Since there must be two data reads per processing cycle, the only power savings in the data storage RAM is in the reduced device size due to an increased allowable access time. The main savings in power is in the coefficient storage RAM and in the multiplier-accumulator portions of the filter, each of which operates at half the clock rate of (1).

B. Low Power RAM Design

A preliminary 6-transistor RAM cell has been designed and laid out using SOS III design rules. Accurate parasitics have been extracted from this layout for use in power dissipation calculations and performance simulations (see Figure 2). Worst case circuit simulations at 85 degrees have shown that the 250-ns access time requirement can be met using minimum geometry devices ($W_n=W_p=2\mu m$). The RAM cell size is 35.4 μm x 27.6 μm, which means that the portion of this chip occupied by just these cells, not the full RAM, is 27.9k mil^2 (167 mils on a side)

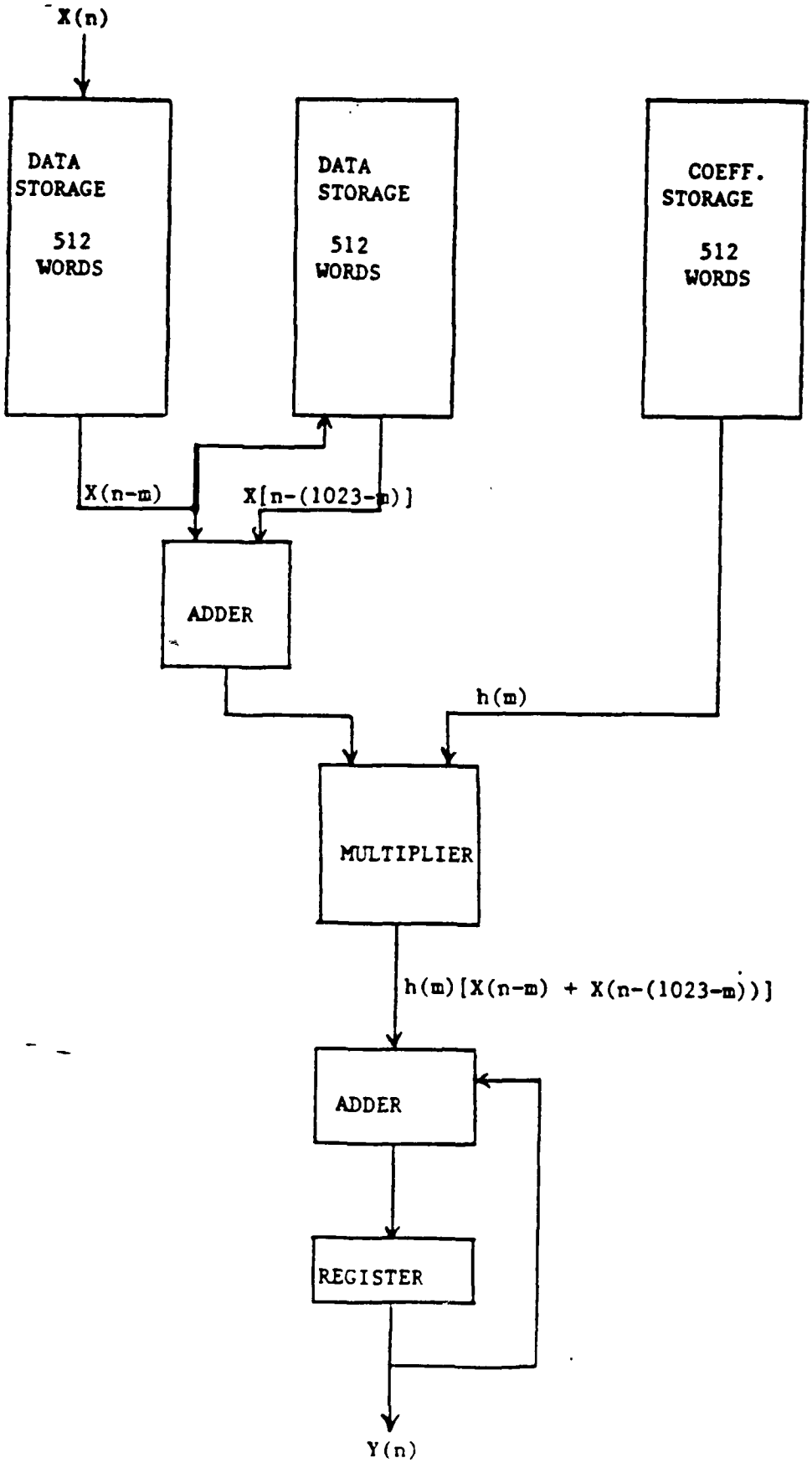
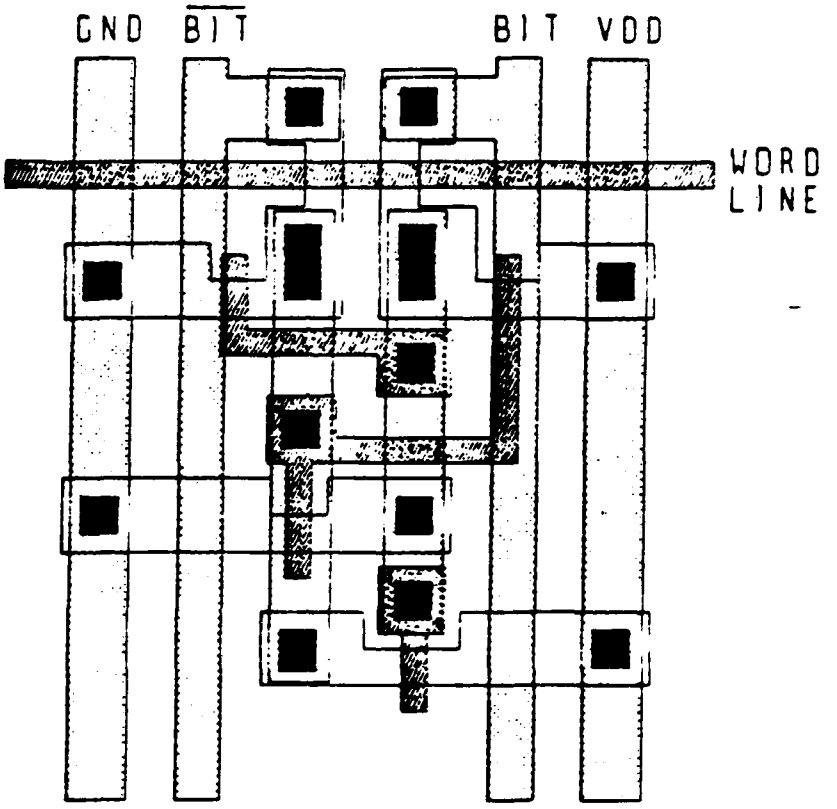


Figure 1. Low power implementation of equation (2).



6-T RAM CELL (27.6UM X 35.4UM)

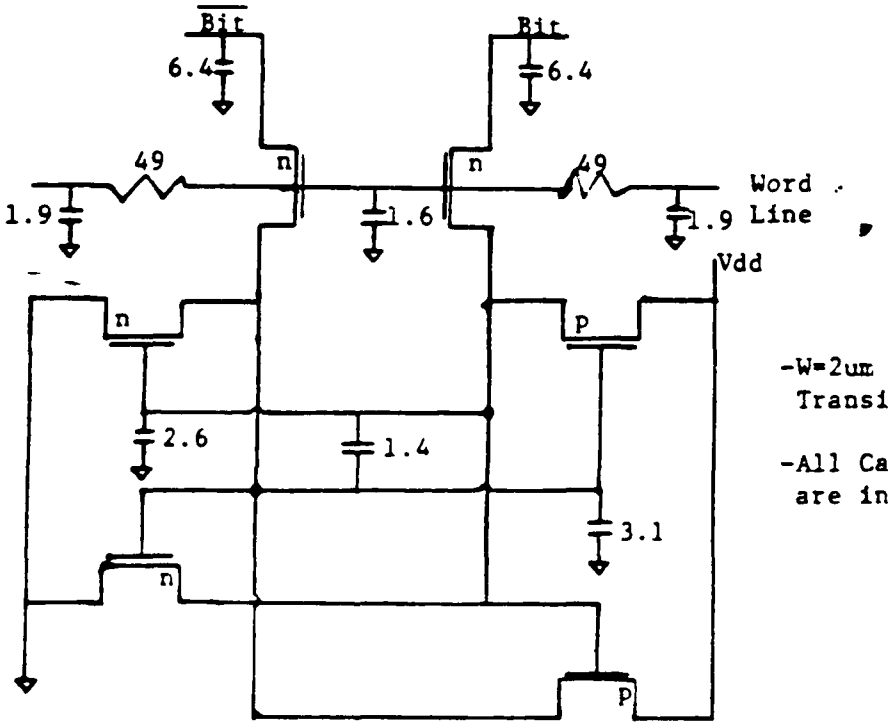


Figure 2. 6-T RAM Cell Layout and Corresponding Circuit

As illustrated in Figure 3, the RAMs are divided into two halves, each containing four sections of 12-bit data words. In a standard RAM, when a particular word is addressed, eight words would be presented to the column decoder which would choose one of the eight. This means that 8 x 12 = 96-bit lines switch with each new address. Since 96 lines are switching and only 12 are accessed, the power dissipated by the other 84 lines is wasted. Two techniques are presented below which are designed to reduce the number of transitioning bit lines to the theoretical minimum of 12 bit lines per new address.

The first technique to reduce the number of transitioning bit lines can be seen in Figure 4a. The row decoder's word lines are ANDed with an enable signal (A8) so that the activated word line is disabled on one side of the RAM while passing unaltered on the other side. This reduces the number of transitioning bit lines in half and hence also reduces the power dissipation associated with bit line switching by one half. The power associated with driving the word line is also cut in half. An additional technique is illustrated in Figure 4b. Here, the sections which are not selected have their bit lines precharged low rather than high. When the word line becomes active, the bit lines are only driven to Vdd-Vt. Since power dissipation is proportional to voltage squared, a reduction of more than half ($2.4^2/3.6^2 = .44$) is realized with a supply voltage of 3.6 V.

Simulations have shown that the dominant power dissipation component in the above described RAM is the transient component given by CV^2F where C = the load capacitance driven to a voltage V once every 1/f seconds. Note that if a line is carrying data,

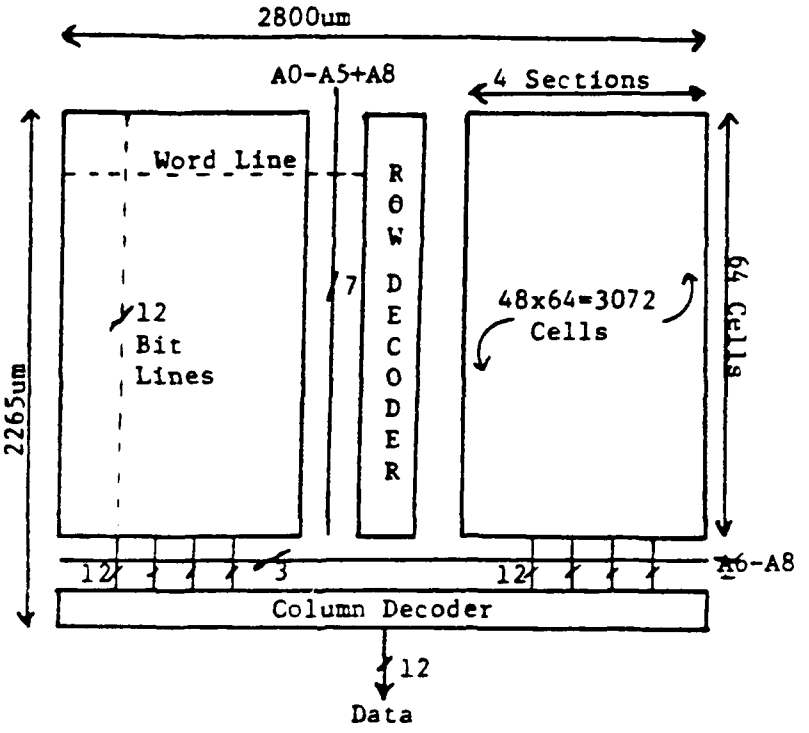


FIGURE 3: 512 Word RAM Configuration.

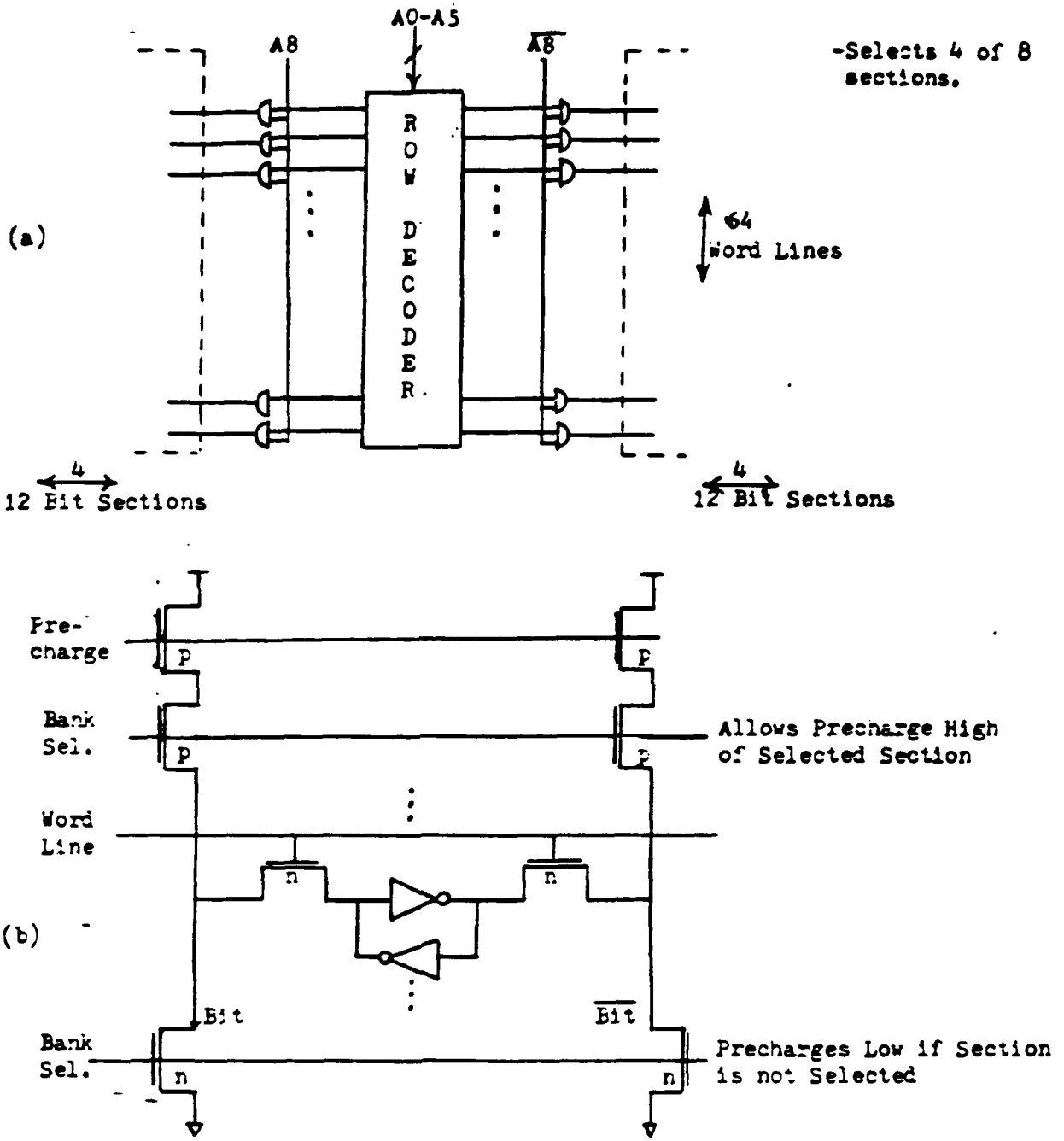


Figure 4: Two Methods For Reducing RAM Power Dissipation.

the maximum signal frequency of that line will occur when alternating bit sequences are present. This means a data rate of 1/4 MHz = 250 ns will produce a signal where two rising edges are separated by a minimum of 500 ns. Thus, although the processing rate is 4.1 mHz, the frequency used in the CV^2F calculations is 2.05 mHz.

There are four main contributors to the power consumption in a RAM: the address lines, the word lines, the bit lines, and the data lines. The capacitance associated with each is outlined below:

-Address lines: 7 lines ● 2265 μm -> 2.54 pF
3 lines ● 2800 μm -> 1.35 pF
Total -> 3.89 pF

-Word lines: 4 x 12 = 48 cells ● 10.2 fF/cell
Total -> 0.49 pF

-Bit lines: 12x64 = 768 cells ● 7.5 fF/cell -> 5.75 pF ● 3.6 V
3x12x64 = 2304 cells ● 7.5 fF/cell -> 17.25 pF ● 2.4 V
(Uses full 4-mHz rate since bit lines are precharged.)

-Data lines: 12 lines ● 2800 μm -> 5.38 pF

A 12-bit register is required to hold the RAM address. The power dissipated by this register is tabulated in Section C. Using the above data, the total power dissipation for the three RAMs is:

$$P_{ram} = 3.02 \text{ mW}$$

C. Multiplier-Accumulator, Adder, I/O, Leakage

The present VHSIC standard cell library consists of cells designed with an emphasis on speed and area. A redesign of the adder cell and D-flipflop cell will be required to reduce the power dissipation of these cells. The following table summarizes

the performance and power tradeoffs of a 12-bit adder and register cell with nominal loads (derived via circuit simulations):

	Before Redesign		After Redesign	
CELL	Delay	Power	Delay	Power
12-bit adder	45 ns	127 μW	95 ns	33.6 μW
12-bit register	6 ns	255 μW	17.2 ns	83.2 μW

The multiplier configuration chosen is a pipelined Booth multiplier. If a sign-magnitude format is used, the multiplier must multiply two 11-bit numbers. The estimated size of the multiplier using VHSIC standard cells is 1963 μm x 1950 μm. Using this data, estimates were made for the lengths of the various interconnect lines required for the multiplier. The total capacitance of all these lines is estimated to be 13.2 pF which dissipates 346 μW of power. There are five rows of registers presenting a combined load (including interconnect parasitics) of 6.1 pF requiring 320 μW of power. The number of adder and register cells is known from [1]. The power dissipation associated with each cell is known from the above table. An estimate was made of the power dissipation for the select circuits. The total power dissipation for all these cells was estimated to be 781.6 μW which includes parasitic capacitances. Thus, the total power dissipated by the multiplier, including interconnect capacitances, is:

$$P_{mult} = 1.45 \text{ mW}$$

The accumulator circuit consists of a 22-bit adder and a 22-bit register. The outputs of the register must drive the 12 data output buffers. However, the power associated with these lines is negligible since they are driven at 8 kHz. Thus, the total power of the accumulator circuit can be derived from the above table:

$$\boxed{P_{acc} = 215\ \mu W}$$

A 12-bit adder is used to sum the two data samples before being multiplied by a filter coefficient. The outputs of this adder may have to drive a significant load because the interconnect lines must connect these outputs to the multiplier. The length of the 12 output lines was estimated so that a capacitance could be derived. A conservative estimate of 422 fF per output line was derived which requires 132 μW of power for all twelve lines. Two twelve-bit registers will be required to hold the two data samples from the data RAM. The power dissipated by the registers and the adder is derived from the above table as 200 μW. The total power of the adder is therefore:

$$\boxed{P_{add} = 332\ \mu W}$$

Assuming that the input buffers are not TTL compatible and they operate at 8 kHz, their power dissipation is negligible. There

are 12 output buffers, each of which drives 20 pF at 8 kHz. Figure 5 illustrates the buffer design. This buffer was simulated to obtain the crossover (short circuit) current contribution to the total current. A power dissipation estimate of 1.1 μW per output buffer was derived. Thus, for all twelve buffers, the total power consumed is:

$$\boxed{P_{buf} \approx 13.2\ \mu W}$$

The leakage current for SOS III devices operating with V_{ds} = 3.6 V is Iln = 36 pa/μm and Ilp = 72 pa/μm. The pass transistors in the RAM cell do not contribute to the leakage current since they do not occur in complementary pairs. There are about 37,000 pass transistors in the three 512-word RAMs. Assuming a total transistor count of 145,000 (see introduction), this leaves 108,000 transistors. Assuming an average width of Wn=Wp=4μm, the average leakage current is 11.7 μA. This gives rise to a total power dissipation of:

$$\boxed{P_{leak} = 42\ \mu W}$$

D. Total Power

The total power dissipation for the digital filter portion of the hip is given by the following equation:

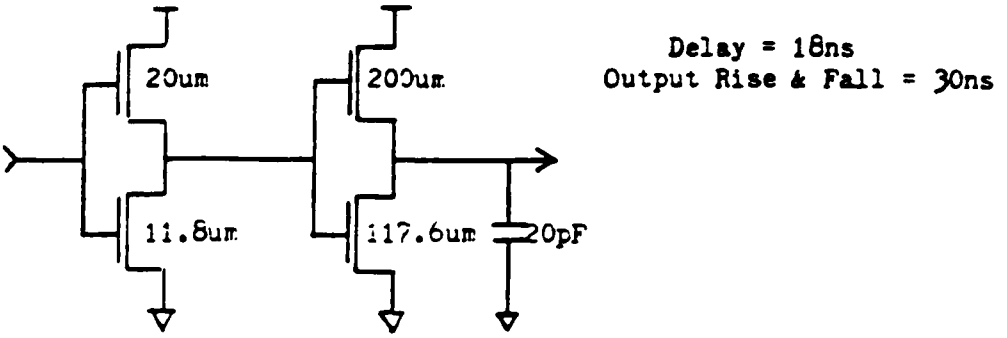


FIGURE 5: 20pF low power output buffer design.

$$P_{tot} = a(P_{ram} + P_{mult} + P_{add} + P_{acc} + P_{buf} + P_{leak}) \quad (3)$$

Assuming that the quantity inside the parenthesis of (3) accounts for 85% of the total power dissipation, the parameter "a" would be 1.15. The extra 15% is for the control circuitry and for the 8 kHz circuitry not included in this analysis. The total power dissipation of the 12-bit digital filter is therefore:

$$\boxed{P_{tot} = 5.8 \text{ mW}}$$

E. A/D Converter

1. Introduction

This section presents an estimate of the power consumption and area of a low power successive approximation Analog to Digital converter. The proposed A/D performs the successive approximation by redistributing charge on an array of binary weighted capacitors. Power estimates are presented based on ISPICE circuit simulations using nominal, room temperature SOS III circuit parameters. Power dissipation estimates associated with the charging and discharging of the capacitor array are based on a preliminary layout of the array.

2. Circuit

A schematic of the proposed charge redistribution A/D implementation is shown in Figure 6. It consists of thirteen binary weighted capacitors, a comparator, and a number of transistors that control the voltages applied to the capacitors. The control and sequencing circuitry are not shown and are not

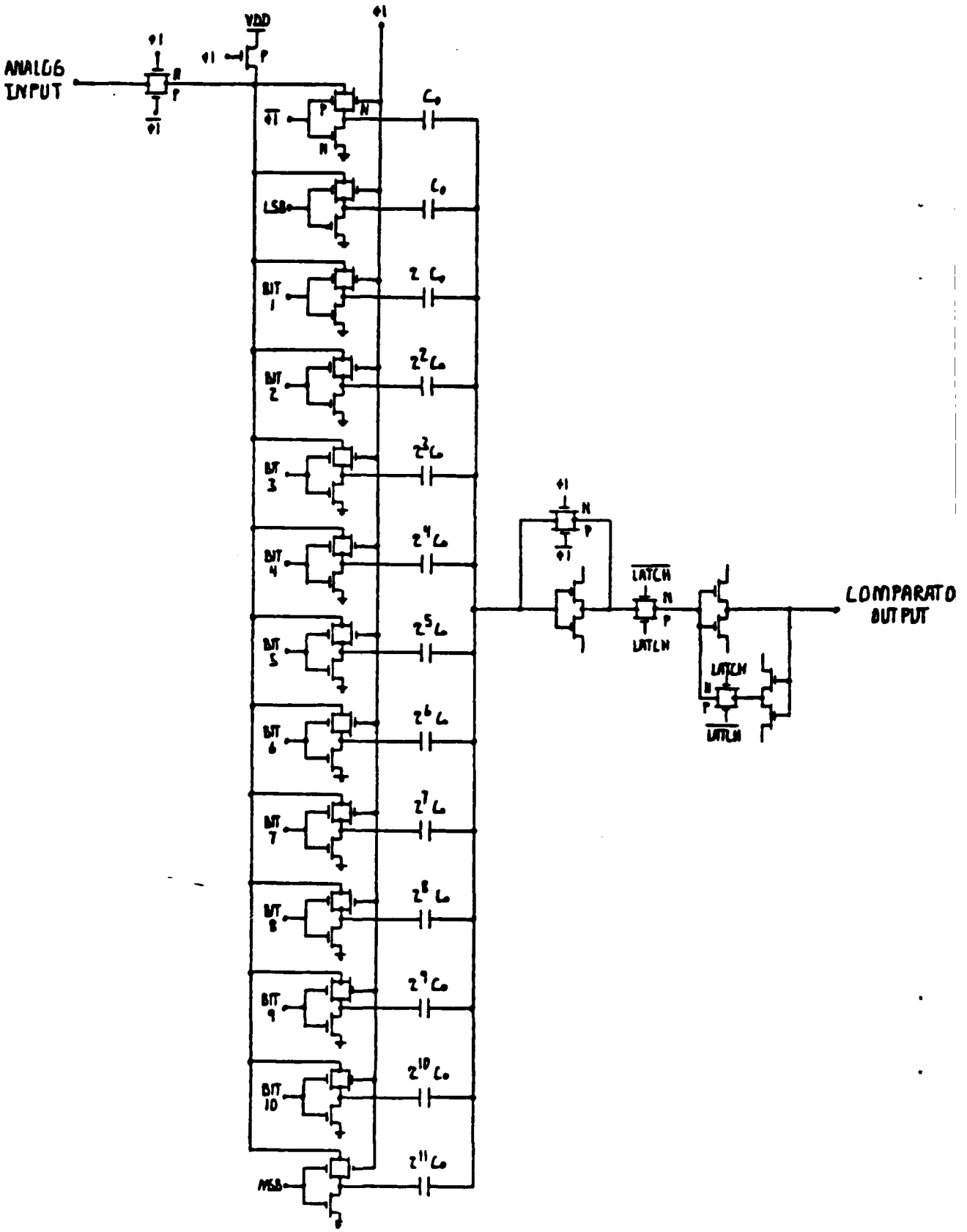


Figure 6. Circuit for successive approximation A/D.

included in the power estimates presented. The A/D conversion is performed in three steps. In the Sample mode ϕ_1 goes high and the bit lines go low. This connects the analog input to the left plates of the capacitors and biases the right plates to the switching threshold of the comparator. In the Hold mode ϕ_1 goes low and the bit lines go high, shorting the left plate of the capacitors to ground. This stores a charge on the capacitor array proportional to the sampled analog input. During the Redistribution mode the bit lines are brought low one at a time, and the resulting voltage swings are sensed by the comparator, latched and encoded. For a detailed description of the conversion algorithm please see Reference [3].

3. Comparator

The comparator used in the proposed implementation is a CMOS inverter followed by a D-type latch. The frequency response of the inverter and of the entire comparator is presented in Figure 7. The voltage gain of the inverter is 27dB. The gain of the comparator is 81dB. The nominal power consumption of the comparator when biased at its switching threshold is 2.024 mW. Any mismatch between the inverter and the latch will result in a DC offset in the switching threshold of the comparator. Another source of DC offsets is the charge dumped onto the capacitor array by the transistors in the transmission gate when they are turned off. It is assumed that in the voice band filtering application that this A/D will be used; the absolute dc level of the encoded signal is unimportant. In this case the only adverse effect of a DC offset in the comparator will be an apparent clipping of the encoded output if

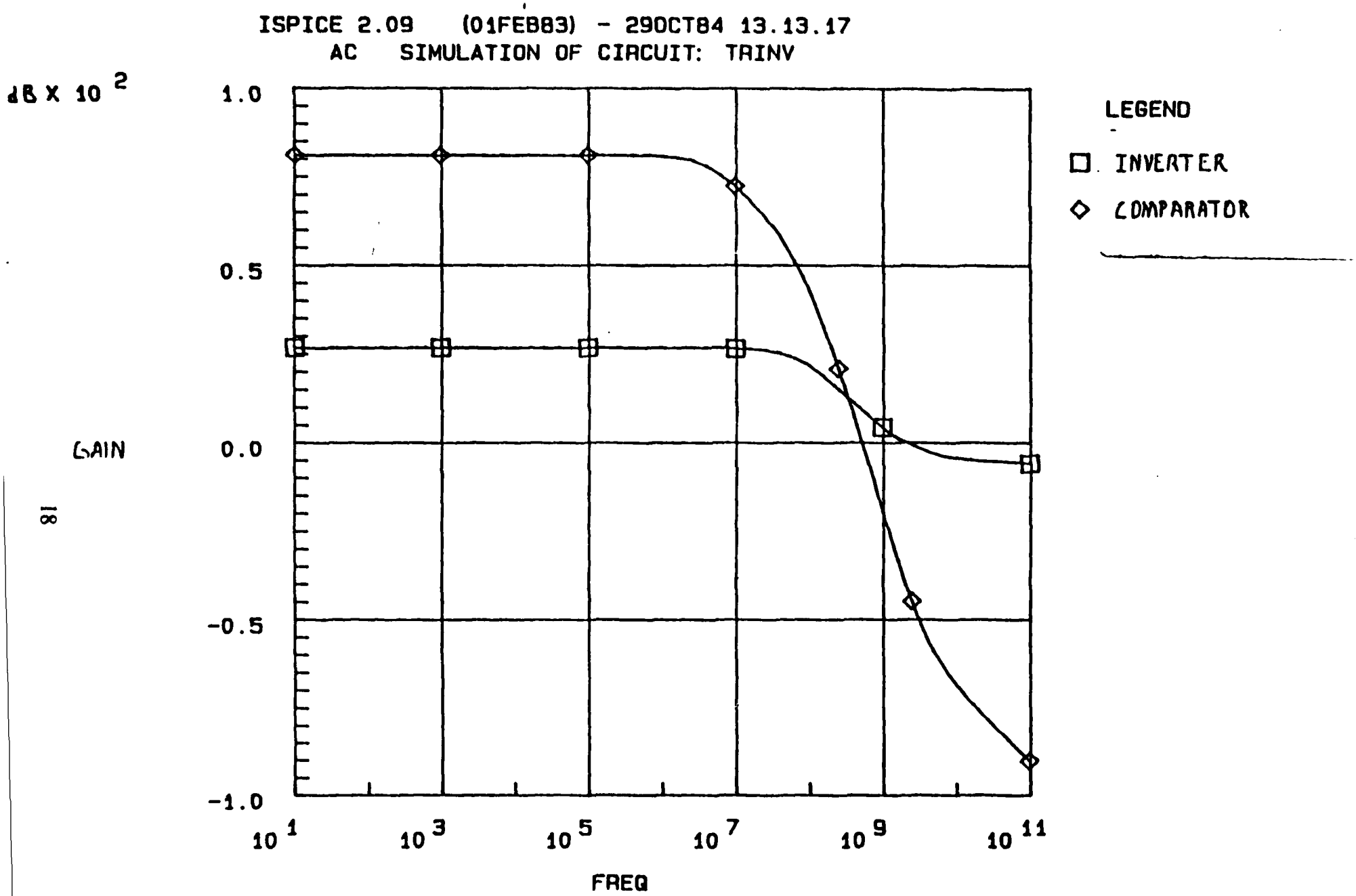


Figure 7. Frequency response of inverter and comparator.

the analog input swings too near the supply rails. Investigation of alternative comparator designs which further cancel the offsets is continuing.

During the Sample mode the analog input is sampled onto the capacitor array. The sampling time constant is determined by the total array capacitance and the on resistance of the inverter and the input and feedback transmission gates. The circuit shown in Figure 8 was used to simulate the Sample mode of operation. Figure 9 shows the response of the circuit to a 3.6-volt step at the input. This figure indicates that the sampling may be performed in approximately 6 μS.

To determine the response time of the comparator to a LSB input the circuit shown in Figure 10 was simulated. Figures 11 and 12 show the comparator response when the LSB bit control line is toggled. These figures also further illustrate the gain of the comparator.

4. Capacitor Array

A layout and schematic of the unit capacitor cell is shown in Figure 13. Each cell consists of a .2142 fF capacitor and three transistors. When arrayed with the reference line, ground, ϕ_1 and the right plate the capacitor will be common to all cells. The cells have been laid out such that when placed side by side they form a 40.5-μm square. During the Sample mode the bit Control Line goes low, ϕ_1 goes high, and the reference line is connected to the Analog input. Transistors M2 and M3 act as a transmission gate connecting the input voltage to the left plate of the capacitor. If M3 were omitted, then input voltages within a threshold drop of ground could not be transferred to the

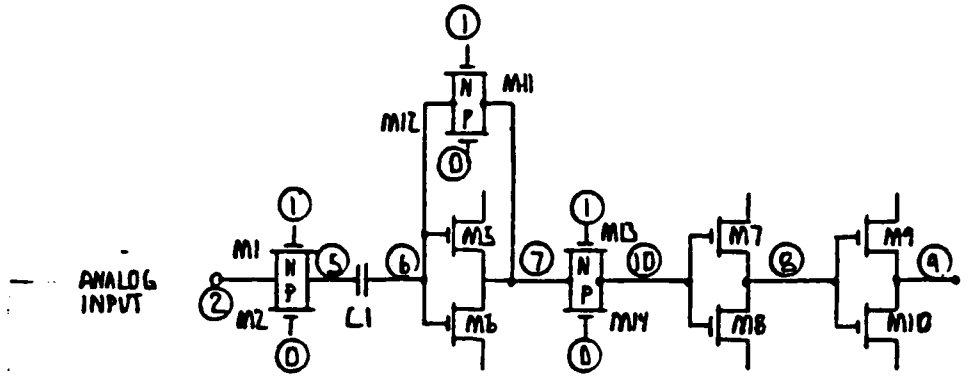


Figure 8. Circuit used to simulate sample mode of operation.

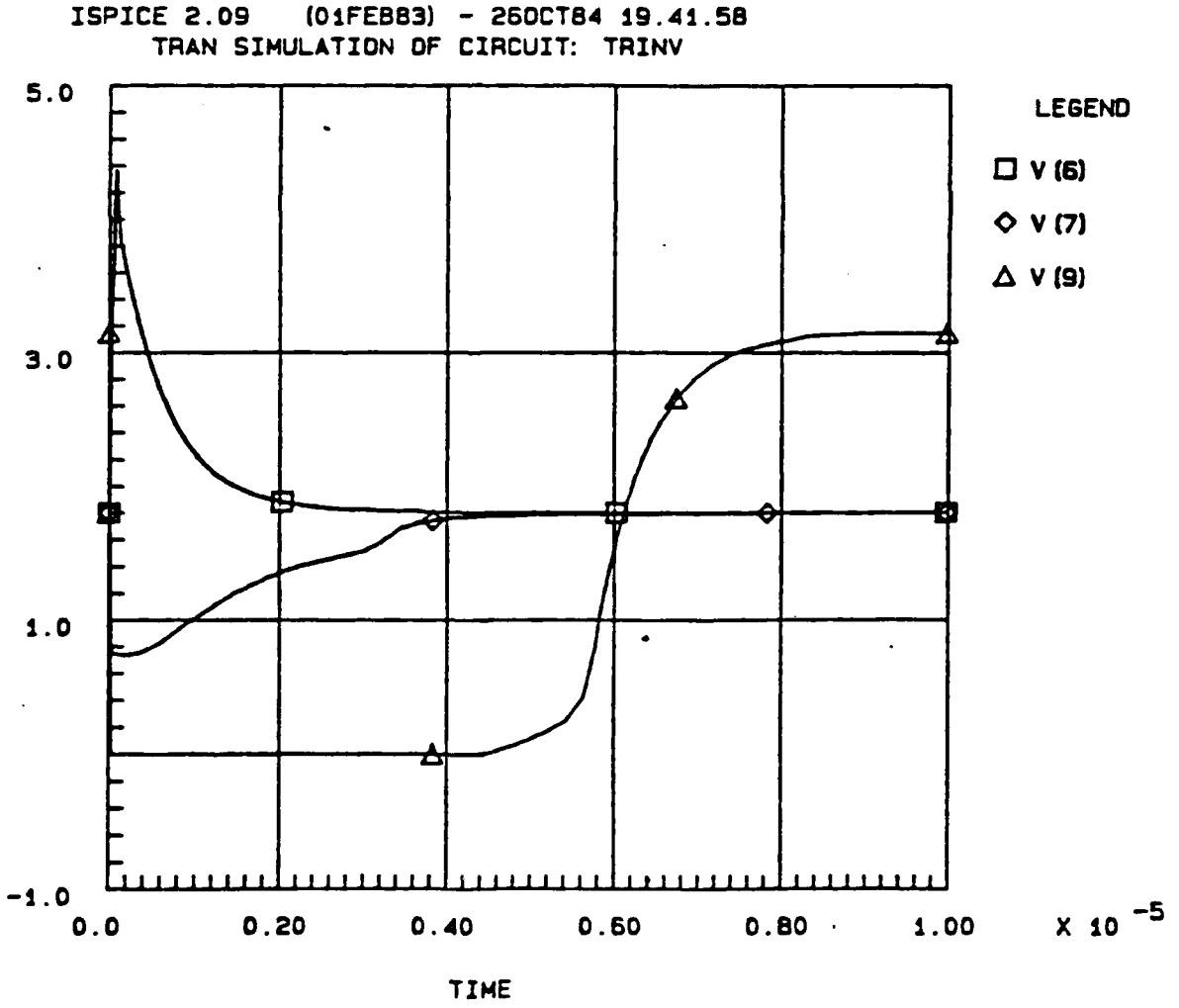


Figure 9. Response time of sampling circuit.

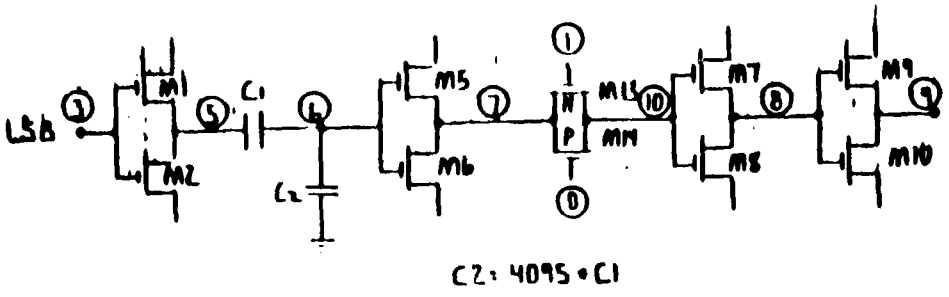


Figure 10. Circuit used to simulate comparator.

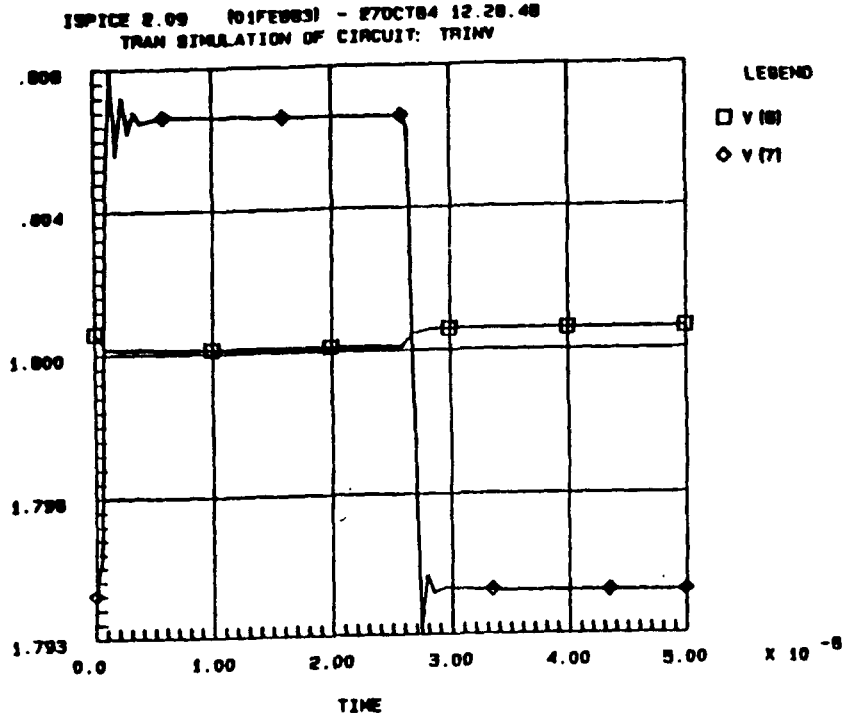


Figure 11. Transient characteristics of comparator response when LSB control line is toggled (blow up).

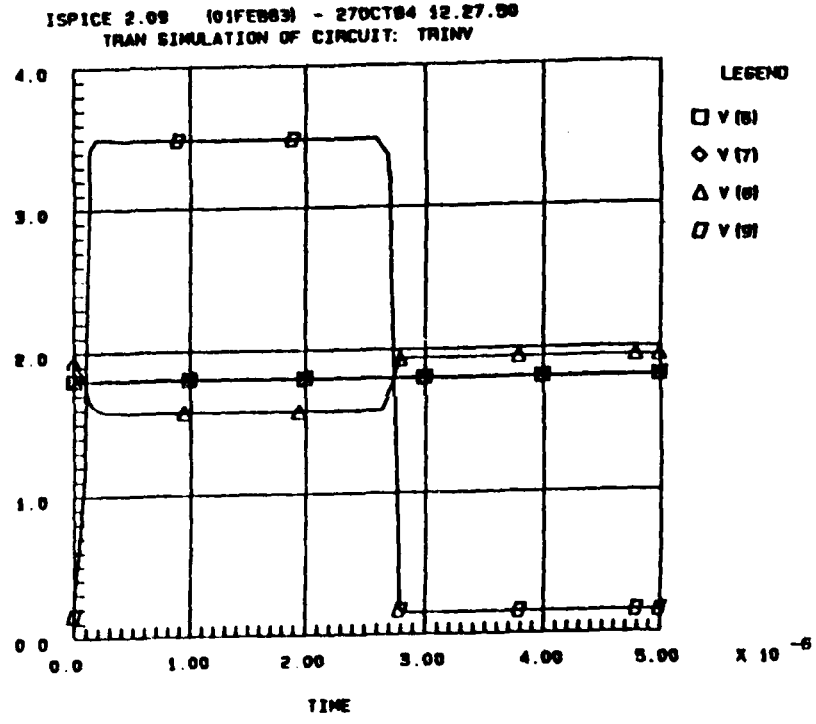


Figure 12. Same as Figure 11 except scale enlarged.

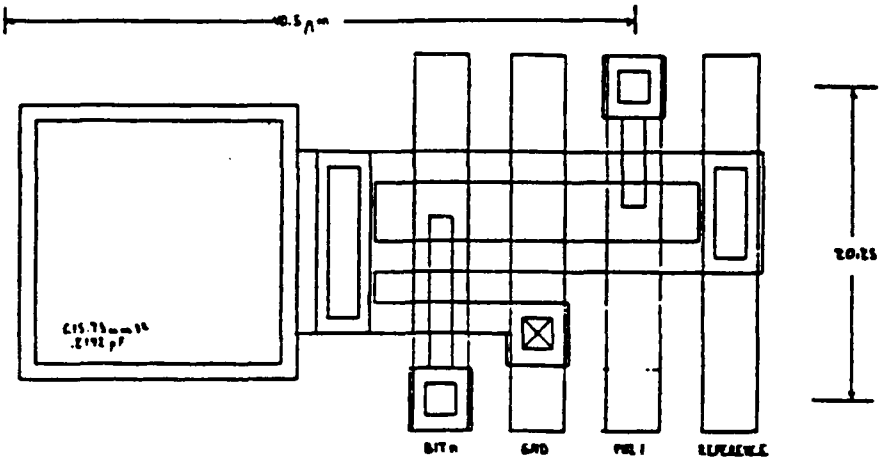


Figure 13. Layout and associated circuitry of single capacitor cell.

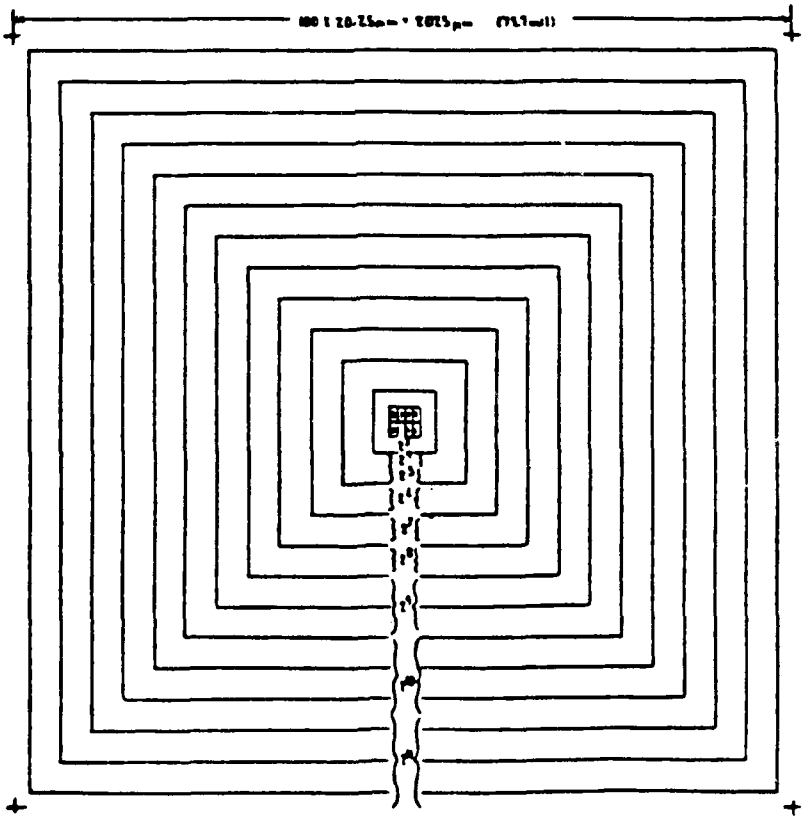


Figure 14. Layout of capacitor array.

capacitor. During the Hold and Redistribution modes ϕ_1 goes low and the reference line is connected to V_{dd}. Transistors M1 and M2 then act as an inverter switching the capacitor plate between ground and V_{dd} under the control of the bit Control line.

An estimate of the area and power consumption of the capacitor array was made using the sample layout shown in Figure 14. The concentric squares represent the reference, ground, and ϕ_1 lines common to adjoining capacitor cells. The layout was formed by adding concentric rings of capacitor cells until the required number of cells for a given bit was reached. No effort was made to optimize the layout by filling empty capacitor cell sites. A capacitor array laid out in this fashion would be 2025 μm (79.7 mil) square. An estimate of the ϕ_1 and bit line capacitances based on these layouts is presented in the following table:

bit	Concentric bit Line Length (cm)	Length to Array Perimeter (cm)	Total Length (cm)	Capacitance (pF)
11	2.14	1.62E-2	2.16	3.01
10	1.56	4.05E-2	1.60	2.24
9	1.16	5.67E-2	1.22	1.71
8	.583	6.48E-2	.648	.907
7	.454	7.29E-2	.527	.738
6	.324	8.10E-2	.405	.567
5	.130	8.10E-2	.211	.295
4	6.57E-2	8.91E-2	.155	.217
3	6.57E-2	8.91E-2	.155	.217
2	8.10E-3	9.72E-2	.105	.147
1	8.10E-3	9.72E-2	.105	.147
0	8.10E-3	9.72E-2	.105	.147
			Total	10.34 pF

Where C=length*1.34pf/μm from reference using W=3.5 μm and S=2.75 μm.

The capacitive load of each transistor including parasitics is 4.80 fF. The total capacitive load seen by the bit Control line and ϕ_1 drivers is given by:

Load	bit Line	ϕ_1
Interconnect	10.34 pF	10.34 pF
Transistor	39.32 pF	19.66 pF
Total	49.66 pF	30.00 pF

Each bit line changes state four times during a conversion--twice during the sample mode and twice during the redistribution. Therefore the frequency used in the power calculation is 2*8kHz=16kHz. The ϕ_1 line toggles at 8kHz. The bit line and ϕ_1 power consumption is given below.

bit Line	10.30 μW
ϕ_1	3.11 μW
Total	13.41 μW

To calculate the power dissipated charging and discharging the capacitors we must consider the sample and redistribution modes separately. During the sample mode all of the capacitors switch together and the power is given by

$$CV^2F = 4096*Co*(3.6)^2*8E3$$
$$= 90.97\ \mu W$$

During the redistribution mode load capacitance being switched is the nth capacitor in series with the remaining capacitors.

$$Cl(n) = \frac{Cn * (CT - Cn)}{CT}$$

$$= Cn - \frac{Cn^2}{CT}$$

Since each bit line is queried once during the A/D conversion we may add the effective load capacitances together to compute the power dissipation. The effective load is given by:

$$Cl = \sum_{n=0}^{11} Cn - \frac{Cn^2}{CT}$$

$$= \sum_{n=0}^{11} 2^n * Co - \frac{2^{2n} * Co^2}{4096*Co}$$

$$= 2730.7 * Co$$

The power dissipated switching this capacitance is given by

$$CV^2f = 60.64\ \mu W.$$

The final area of power consumption related to the capacitor array is the leakage of the transistors in each unit cell. The worst case leakage condition is during the hold mode when the bit lines are high and ϕ_1 is low. In this case there is a leakage current in transistors M2 and M3 of the unit cell. Using leakage currents of Iln=36pA/μm and Ilp=72pa/μm the power dissipated is given by:

$$P = 4096 * [2\mu m * (36\ pA/\mu m + 72\ pA/\mu m)] * 3.6\ V$$

$$= 3.19\ \mu W.$$

5. Total Power

The power dissipation of the complete circuit is summarized in the following table:

Source	Power 9mW)
Comparator	2.024
ϕ_1 and bit lines	.0134
Leakage	.00319
Capacitors	
Sample Mode	.09097
Redistribution Mode	0.06064
Total	2.192 mW

It is assumed that the control and sequencing circuitry will not significantly increase the total power dissipation.

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